REMARKS

At the outset, the Examiner's attention is directed to the Substitute Specification (Marked-Up and Clean versions) submitted concurrently herewith. The specification has been amended to provide the correct statement with regard to the benefit of the earlier filing of the present application under 35 U.S.C. §120. The specification has also been amended so that reference numerals 28 and 30 refer to DC paths, as requested in item 2, page 2 of the Office Action.

The allegation in item 2, page 2 that DC paths and DC connections are improper is incorrect. A DC path or DC connection, in many cases, carries an AC signal, i.e., voltages and currents that change. In fact, all DC paths and DC connections are capable of carrying AC variations. A common circuit, known as a DC coupled amplifier, has DC paths or DC connection that carry signals having a spectrum between DC and into the megahertz or the gigahertz ranges, see enclosed Exhibits A and B, respectively copies of U.S. Patent 6,218,838 and an advertisement by RF Bay, Inc. for a 0 Hz – 17 MHz DC coupled amplifier. In '838, note the DC to gigahertz range mentioned at column 1, line 19, and the DC paths of Figure 3. The Examiner is requested to supply support for his position that a DC path or DC connection cannot carry a voltage signal that has transitions or swings between ground and a supply voltage.

Applicants have amended claims 5, 6, 9 and 15 to overcome the objections in the third, fifth, sixth and ninth paragraphs on page 3 of the Office Action, and amended claim 1 to assure infringement when the goods are sold, prior to being put to use.

The Examiner, in objecting to claim 3, line 2 and claim 9, line 3, is attempting to narrow Applicants' protection through the use of informalities. The DC voltages applied to the switchable capacitors are not necessarily the power supply voltages that are applied the across the series connected source drain paths of the first and second transistors specified in the claims. For

example, the DC voltages applied to the switchable capacitor electrodes could be the same, greater, or less than the voltages of the power supply terminals. The test to determine a proper rejection of a claim under 35 U.S.C. §112, paragraph 2, is whether a member of the public is able to determine if a device infringes or a planned device will infringe a claim. There is no requirement for a claim to have every connection specified in the drawing, as implied in the Office Action. If the Examiner repeats the objection to claims 3 and 9, he is requested to provide support for his position.

Applicants note claims 20 and 21 are indicated as containing allowable subject matter.

To provide applicants with the protection to which they are indeed are entitled, claims 25-27 are added. Claim 25 depends on claim 9, and defines specific connections between the electrodes of the switchable capacitors, and the first and second field effect transistors. Claims 25-27 define the relationships of the circuit elements of Fig. 1, and the operation of Figure 2, in detail.

To overcome the double-patenting rejection, Applicants submit herewith a Terminal Disclaimer signed by an attorney of record.

In response to the rejection under 35 U.S.C. §112, paragraph 2, claim 5 has been amended to cure the indefiniteness pointed out in the third paragraph at page 3 of the Office Action.

Claim 7 has been amended to obviate the rejection thereof under 35 U.S.C. §112, paragraph 2, in the paragraph of the Office Action bridging pages 5 and 6. Claim 7 now more clearly indicates the second electrode is connected to the same power supply terminal that supplies current to the NFET second source drain path, while the NFET second transistor drain path is on. For example, in the specific embodiment, this means the common source drain connection of switchable capacitor 32 is connected to ground terminal 18, that supplies current to the source drain path of NFET 50, while NFET 50 is on and PFET 40 is off.

The rejection of claim 1 for the use of the words "threshold level" on line 5, and "threshold voltage" on line 15 is traversed. Applicants purposely used different terminology in connection with the thresholds of the first and second transistors and the threshold of the capacitor. The recitation of threshold level on line 5 refers to the threshold levels of the first and second transistors, while the threshold voltage on line 15 refers to the threshold of the capacitor. If the same terminology had been used, it is likely the Examiner would have objected to the claim because of indefiniteness and misdescriptiveness because the threshold for the capacitor and thresholds for the transistors differ.

Concerning the use of "DC path" in claim 14, see the prior discussion about the objection to the words "DC path" and "DC connections." If the Examiner persists in this rejection, he must provide rationale as to why DC path, as recited in claim 14, does not read on paths 28 and 30. As discussed *supra*, DC paths can, and most often do, carry changing voltages and currents.

Applicants traverse the rejection of claims 1, 3, 4, 8 and 14-19 as being anticipated by Hamasaki et al. (U.S. Patent 5,694,065). Inspection of the Hamasaki et al. wave forms of Figures 6, 7a and 7b indicates capacitors C_p and C_n do not meet the requirements of independent claim 1 for at least one switchable capacitor arranged to have an initial finite capacitance value during an initial part of a transition, and to be switched from the initial capacitance value to a substantially open circuit in response to the voltage across the switchable capacitor changing during the transition from one side of a threshold voltage to a second side of the threshold voltage, wherein the threshold voltage is between first and second levels of a voltage source. The upper series of wave forms in Figure 6 indicates the voltage variations across capacitors C_p and C_n in response to a positive going transition IN at the input of the circuit of Figure 2, while the lower series wave forms indicates the voltage variations across the capacitors in response to a negative going transition. In response to the

positive going transition, the voltages across capacitors C_n and C_p, respectively indicated by wave forms D01 and D02, change gradually, in the usual manner. There is no sudden change in the voltages of wave forms D01 and D02 as would occur if C_n and/or C_p were switched as required by claim 1.

An inspection of the wave forms of Figures 7A and 7B under the heading "Present Invention" also indicates the voltages across capacitors C_p and C_n do not meet the previously discussed criteria of claim 1.

Further, there is simply no basis for the Examiner to conclude that capacitors C_p and C_n of Hamasaki et al. are switchable, as set forth in claim 1. The Examiner ignores the fact that the thresholds of switchable capacitors can be controlled, and that the wave forms of Figures 6 and 7 indicate the capacitors of Hamasaki et al. are such that they do not meet the criteria of claim 1.

Applicants traverse the rejection of claims 1, 3-9, 11-17 and 22-24 as being anticipated by Bui et al. (U.S. Patent 6,201,752). The Office Action includes numerous unsupported allegations concerning the Bui et al. reference. For example, the Office Action assumes there are a CMOS transistor and an NMOS transistor in inverter 809 of Bui et al. This is not necessarily the case because inverters can be formed by a single transistor. In addition, the Office Action assumes that, during a transition of an input voltage, the two phantom FETs in inverter 809 are activated so they are not simultaneously on. The Examiner has not shown either of these features of claim 1 is necessarily found in Biu.

The most glaring deficiency about the rejection of independent claims 1 and 22 based on Bui et al. is that Bui et al. has no disclosure of FET capacitors 807 and/or 808 being switchable, as recited in claims 1 and 22, and discussed in connection with the rejection based on Hamasaki et al. The Examiner must provide rationale as to why the type of wave forms illustrated in Figures 6, 7a

and 7b of Hamasaki et al. do not occur in Bui et al. The switchable capacitors defined by claim1 have thresholds that are not described by Bui et al. The Examiner must provide rationale to support his view that the limitations recited in the last nine lines of claim 1 are met by the operation of Figure 8A of Bui et al. There is no description in Bui et al. of the operation of the circuit 8A, other than to state it provides delay. The allegation in the first paragraph at page 8 of the Office Action that the operations set forth in the last five lines of claim 9 are inherent in the Bui et al. capacitors because these capacitors are similar to applicants' capacitor is not a correct basis. There is nothing in Bui et al. to indicate capacitors 808 and 807 have thresholds as required by claims 1 or 9. Bui et al. also does not disclose the operating method of claim 22, that requires the first and second capacitors to be switched off, or the structure of new claim 26 that defines the thresholds of the switchable capactiors and details about the operation of the circuit..

The Examiner has not met the criteria for a proper rejection based on inherency. If the Examiner is stating that the quoted portion of Bui et al. inherently includes the first and second capacitors that meet the requirements of the last nine lines of claim 1, and the similar language of claim 22, the Examiner has not met the burden of establishing a *prima facie* case of inherency. The fact that a certain result or characteristic ***may*** occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). To establish inherency, extrinsic evidence must make clear that the missing descriptive matter is ***necessarily*** present in the thing described in the reference and that it would be so recognized by persons of ordinary skill in the art. Inherency may not be established by possibilities or probabilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *In re Roberston*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51

(Fed. Cir. 1999). In relying upon a theory of inherency, the Examiner must provide a basis in fact or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (B.P.A.I. 1990). Because there is no mention in Hamasaki or Biu et al. of the switchable capacitors and the thresholds recited in the claims, the similarity of applicants' circuit diagram to the circuit diagrams of Hamasaki and Bui is irrelevant. Since the Examiner has not provided rationale or evidence to show that Bui et al. and Hamasaki inherently provide the requirements of the independent claims, the rejections of the independent claims based on Bui et al. and/or Hamasaki are incorrect and must be withdrawn.

In view of the foregoing amendments and remarks, favorable reconsideration and allowance are in order.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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